I claim:

1. A differential comparator system, comprising:

first and second strings each formed with at least one impedance element;

at least one current source coupled to a first end of at least one of said first and second strings;

at least one comparator coupled to provide a comparator output signal in response to signals at first and second string taps that are respectively positioned along said first and second strings; and

first and second differential amplifiers that have first input terminals which together define a differential input port, that have second input terminals that are each coupled through a respective feedback path to a feedback tap positioned between the first and second ends of a respective one of said first and second strings, and that are each coupled to drive a second end of a respective one of said first and second strings;

said system thus providing a comparator output signal in response to input signals at said differential input port.

2. The system of claim 1, further including first and second pass transistors each inserted between a respective one of said first and second differential amplifiers and that amplifier's respective second end.

3. The system of claim 1, wherein:

said first and second strings each comprise a plurality of serially-coupled impedance elements; and

at least one comparator comprises a plurality of comparators coupled to each provide a portion of said comparator output signal in response to respective first and second taps that are respectively positioned along said first and second strings.

4. The system of claim 1, wherein said at least one current source comprises a first current source coupled to the first end of said first string and a second current source coupled to the first end of said second string.

5. The system of claim 1, wherein said impedance elements are resistors.

6. The system of claim 1, wherein each of said differential amplifiers includes;

first and second diode-coupled transistors;

a current source that provides an amplifier current; and

a differential pair of transistors that provide said first input terminals and that are coupled to steer said amplifier current to said first and second diode-coupled transistors in response to said input signals.

7. An analog-to-digital converter, comprising:

first and second strings each formed with at least one impedance element;

at least one current source coupled to a first end of at least one of said first and second strings;

at least one comparator coupled to provide a comparator output signal in response to signals at first and second string taps that are respectively positioned along said first and second strings;

first and second differential amplifiers that have first input terminals which together define a differential input port, that have second input terminals that are each coupled through a respective feedback path to a feedback tap positioned between the first and second ends of a respective one of said first and second strings, and that are each coupled to drive a second end of a respective one of said first and second strings; and

a decoder coupled to provide an output digital code in response to

said comparator output signal;

said converter thus providing an output digital code in response to input signals at said differential input port.

8. The converter of claim 7, further including first and second pass transistors each inserted between a respective one of said first and second differential amplifiers and that amplifier's respective second end.

9. The converter of claim 7, wherein:

said first and second strings each comprise a plurality of serially-coupled impedance elements; and

at least one comparator comprises a plurality of comparators coupled to each provide a portion of said comparator output signal in response to respective first and second taps that are respectively positioned along said first and second strings.

10. The converter of claim 7, wherein said at least one current source comprises a first current source coupled to the first end of said first string and a second current source coupled to the first end of said second string.

11. The converter of claim 7, wherein said impedance elements are resistors.

12. The converter of claim 7, wherein each of said differential amplifiers includes;

first and second diode-coupled transistors;

a current source that provides an amplifier current; and

a differential pair of transistors that provide said first input terminals and that are coupled to steer said amplifier current to said first and second diode-coupled transistors in response to said input signals.

13. A gain-controlled receiver that provides a digital output signal

in response to an analog input signal, comprising:

an amplifier that processes said analog input signal to a level-controlled signal with a gain that varies in response to a feedback signal;

a mixer that provides a downconverted signal in response to said level-controlled signal;

an analog-to-digital converter that converts said downconverted signal to said digital output signal;

a differential comparator system that provides an out-of-range signal when said downconverted signal exceeds a predetermined range; and

a processor that provides said feedback signal in response to said digital output signal and alters it in response to said out-of-range signal;

wherein said comparator system includes:

a) first and second strings each formed with at least one impedance element;

b) at least one current source coupled to a first end of at least one of said first and second strings;

c) at least one comparator coupled to provide said out-of-range signal in response to signals at first and second string taps that are respectively positioned along said first and second strings; and

d) first and second differential amplifiers that have first input terminals coupled to receive said downconverted signal, that have second input terminals that are each coupled through a respective feedback path to a feedback tap positioned between the first and second ends of a respective one of said first and second strings, and that are each coupled to drive a second end of a respective one of said first and second strings.

14. The receiver of claim 13, further including first and second pass transistors each inserted between a respective one of said first and

second differential amplifiers and that amplifier's respective second end.

15. The receiver of claim 13, wherein said at least one current source comprises a first current source coupled to the first end of said first string and a second current source coupled to the first end of said second string.

16. The receiver of claim 13, wherein said impedance elements are resistors.

17. The receiver of claim 13, wherein each of said differential amplifiers includes;

first and second diode-coupled transistors;

a current source that provides an amplifier current; and

a differential pair of transistors that provide said first input terminals and that are coupled to steer said amplifier current to said first and second diode-coupled transistors in response to said input signals.

18. The receiver of claim 13, further including a low-pass filter inserted between said mixer and said converter and wherein said differential comparator responds to a differential signal provided by said filter.

19. The receiver of claim 13, further including an oscillator that provides a local oscillator signal to said mixer.

20. The receiver of claim 13, wherein said processor responds to said digital output signal in the absence of said out-of-range signal.